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| 10/586,549 | 07/19/2006 | Henry Tan | P/2778-84 | 6234 |

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| EXAMINER | |
|---|---|
| YU, JAE UN | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/586,549 | TAN ET AL. | |
| | Examiner | Art Unit | |
| | JAE U. YU | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/19/06, 2/19/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

The examiner acknowledges the applicant's submission of 10586549 dated 7/19/2006. At this point claims 1-20 are pending in the instant application.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 5** recites the limitation "the control data storage sector". There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (US 5,404,485) in view of Higuchi et al. (US 2002/0120820), referred to as "Higuchi" hereinafter.

2. As per **independent claim 1**, Ban discloses; "a data interface for transferring data packets into and out of the device, an interface controller, a master control unit, and at least one flash memory unit, the interface controller being arranged to send data received through the interface to the master control unit, and the master control unit being arranged to recognise certain data packets as encoding READ instructions and other data packets as encoding WRITE instructions: **[Figure 1 & Figure 6]**",

"upon receiving a READ instruction indicating a logical address, to access a memory address mapping table **[Figure 3]** which associates logical address regions within a logical memory space with respective first physical address regions within the memory unit, to read data from a physical address in the memory unit **["Physical Address", Figure 5]** corresponding to the logical address **["Virtual Address", Figure 5]** according to the address mapping table, and to transmit to the data interface one or more data packets including the data which was read", and

"upon receiving a WRITE instruction indicating a logical address and data to be written to that logical address, to determine if the physical address corresponding to the logical address according to the memory address mapping table is in the erased state **[Step 47, Figure 6]** and: if so, to write the data to that physical address **[Step 49, Figure 6]**, or if not, to modify the address mapping table to associate a second physical address region with the logical address region containing the logical address **[Step 53 & 54, Figure 6]**, to write the data to a physical address corresponding to the logical address

according to the modified memory address mapping table **[Step 52, Figure 6]**, and to copy any data stored in other potions of the first physical address region to corresponding locations of the second physical address region **[Figure 7 & 8]**".

Ban does not disclose expressly that the flash memory unit is a "NAND flash memory".

**Higuchi discloses a NAND flash memory in paragraph 7.**

Ban and Higuchi are analogous art because they are from the same field of endeavor of flash memory control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ban by including a NAND flash memory as taught by Higuchi in paragraph 7.

The motivation for doing so would have been "a large capacity, small size, and low power consumption" as expressly taught by Higuchi in paragraph 7.

3. As per **claim 2**, "data defining the memory address mapping table is stored as mapping data in the flash memory unit **[map stored in the flash memory, Paragraph 3]**, the memory control device being arranged to modify the mapping data upon modifying the memory address mapping table **[Figure 3 & 6]**".

4. As per **claim 3**, "the memory control address unit is arranged, upon being initiated, to extract the mapping data from the flash memory unit **[map stored in the flash memory, Paragraph 3]** and generate the memory address mapping table within RAM memory **[map stored in random access memory, Paragraph 3]**".

5. As per **claim 4**, "the portion of the mapping data defining the mapping between each respective physical address region and a logical address region is stored within that physical address region **[Figure 3]**".

6. As per **claim 5**, "the mapping data relating to a given physical address region is stored in the control data storage sector of one or more pages of the physical address region **[Figure 3]**".

7. As per **claim 6**, "physical memory regions associated with logical address regions by the memory address mapping table **[Figure 3 & 4]**, and queuing physical memory regions which can become associated with the logical addresses under the operation of the master control unit which modifies the memory address mapping table **[Figure 3 & 4]**".

8. As per **claim 7**, "the queuing physical memory regions are in the erased state **[Figure 6]**".

9. As per **claim 8**, "reserved physical memory regions **["Transfer Unit", Figure 7]** which cannot become associated with the logical addresses under the operation of the master control unit which modifies the memory address mapping table".

10. As per **claim 9**, "the physical address regions are respective blocks of the memory unit **[Figure 3]**".

11. As per **claim 10**, "the physical address regions are groups of blocks in the memory unit, the groups being defined to a grouping table **[Figure 9]**".

12. As per **claim 11**, "the majority of groups of blocks are defined according to a rule, and the grouping table defines groups which are exceptions to the rule **[Figure 9]**".

13. As per **claim 12**, "the memory address mapping table contains a flag in respect to any logical address region which is associated with one of the groups which are exceptions to the rule **[Figure 9]**".

14. As per **claim 13**, "the master control unit associates consecutively following logical addresses within a logical address region **[Element 31, Figure 4]** with respective pages in different ones of the blocks **[Element 35, Figure 4]**".

15. As per **claim 14**, "the master control unit associates consecutive logical addresses into sets **[Element 31, Figure 4]**, each of the sets of logical addresses having a number of members equal to the number of blocks in each group, and for each given set the master control unit associates the logical addresses of that set with corresponding pages of the respective blocks **[Element 35, Figure 4]**".

16. As per **claim 15**, "the master control is arranged, in response to receiving a first WRITE instruction to implement the write instruction only upon determining that **[receiving a first write instruction, Figure 6]**, within a predefined period, a second WRITE instruction is not received obeying a predefined similarity criterion **[no second instruction received, Figure 6]**".

17. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (US 5,404,485) in view of Higuchi et al. (US 2002/0120820) as applied to claim 1-15 above, and further in view of Horn et al. (US 2005/0050273), referred to as "Horn" hereinafter.

18. As per **claims 17 and 18**, Ban and Higuchi disclose the device recited in claim 15.

Ban and Higuchi do not disclose expressly that if two write commands try to access the same memory location, then directs a command to other memory location.

**Horn discloses such two write instructions, wherein each instruction is directed to a different memory location from one other in the abstract.**

Ban, Higuchi and Horn are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ban and Higuchi by holding multiple requests in a queue when the requests cause an access overlap as taught by Horn in the abstract.

The motivation for doing so would have been to alleviate memory access conflicts as expressly taught by Horn in the abstract.

19. As per **claim 19**, "there are a plurality of said selected logical addresses **[Figure 3 & 4, Ban]**".

20. As per **claim 20**, "a pattern recognition unit for recognizing logical addresses encoded in the WRITE instructions which arise with relatively high frequency **[access conflict, Abstract, Horn]**, and for setting said recognized logical addresses as said selected logical addresses **[Figure 3 & 4, Ban]**".

***Conclusion***

A. Subject Matter Considered Allowable

1. **Claim 16** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The primary reasons for allowance of **claim 16** in the instant application is the combination with the inclusion in the claim that "**following a modification of the memory address modification table in relation to a given logical address region, and prior to said copying of the data from the first physical address region to the new second address region, said criterion is whether the second WRITE instruction relates to a logical address corresponding to the location within the given logical address region of the data to be copied, and in the case that such a WRITE instruction is received aborting said copying operation and instead writing data specified by the second WRITE instruction to the location of the second physical address region**". The prior art of record neither anticipates nor renders obvious the above recited combination.

3. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

B. Claims Rejected in the Application

Claims 1-15 and 17-20 have received a first action on the merits and are subject of a first action non-final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae U Yu/

Examiner, Art Unit 2185

8/30/2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185